CLAIMS

What we claim:

1. A method of analyzing timing characteristics of an input/output block of a programmable logic device, the input/output block including:
   a. an input logic element having:
      i. a sequential input-logic-element input terminal connected to an input/output pad;
      ii. an input-logic-element clock terminal; and
      iii. a sequential input-logic-element output terminal; and
   b. an output logic element having:
      i. a sequential output-logic-element output terminal connected to the input/output pad;
      ii. a sequential output-logic-element input terminal; and
      iii. an output-logic-element clock terminal;
      iv. wherein the output logic element is adapted to provide an alternating test signal on the output-logic-element output terminal; the method comprising:
         1) presenting data on the sequential output-logic-element input terminal;
         2) presenting a first clock edge on the output-logic-element clock terminal to latch the data into the output logic element; and
         3) presenting a second clock edge on the input-logic-element clock terminal to latch the data in the output logic element into the input logic element.

2. The method of claim 1, further comprising minimizing the time difference between the first and second clock edges.

3. The method of claim 2, further comprising monitoring the contents of the input logic element to ensure the data is properly stored in the input and output logic elements.

4. The method of claim 2, further comprising determining the minimum difference between the first and second clock edges and subtracting the set-up time of the input logic element from the minimum difference to obtain the clock-to-out delay of the output logic element.

5. A method for measuring timing characteristics of an integrated circuit, the method comprising:

providing a first signal at a data input of a sequential logic element of the integrated circuit;

providing a second signal at the clock input of the sequential logic element, wherein the second signal is related to the first signal;

applying a precise delay to one of the first and second signals with a variable delay circuit of the integrated circuit, the precise delay placing a first edge of the first signal with respect to a second edge of the second signal; and

latching data of the first signal in the sequential logic element.

6. The method of claim 5, further comprising dividing the first signal to generate the second signal.

7. The method of claim 5, further comprising determining an error if the latched data does not match a predetermined value.

8. The method of claim 7, wherein the step of determining comprises catching the error in an error catcher of the integrated circuit.

9. The method of claim 5, wherein the precise delay is a first precise delay, the method further comprising applying a second precise delay to one of the first and second signals with the variable delay circuit, wherein the second precise delay is different from the first precise delay, the second precise delay placing a third edge of the first signal with respect to a fourth edge of the second signal.

10. The method of claim 5, wherein the variable delay circuit is a digital clock manager.

11. The method of claim 10, wherein the digital clock manager comprises a delay-locked loop.

12. The method of claim 5, further comprising determining at least one of a hold time, a setup time, and a clock-to-output delay of the sequential logic element based on the latched data and the precise delay.

13. The method of claim 5, wherein the integrated circuit is a programmable logic device.

14. The method of claim 5, further comprising controlling the precise delay with a tester coupled to the variable delay circuit.

15. The method of claim 14, further comprising monitoring the latched data with the tester.

16. The method of claim 5 wherein the precise delay is a precise negative delay.

17. The method of claim 5, wherein the first and second edges are rising edges.

18. A method for measuring timing requirements of a logic element of a programmable logic device, the method comprising:

delivering a first test signal to a data terminal of the logic element;

delivering a second test signal to a clock terminal of the logic element;

placing a first edge of the first test signal a precise delay relative to a corresponding second edge of the second test signal;

latching data of the first test signal in the logic element under test based on timing of the second test signal;

determining functionality of the logic element based on the latched data;

varying the precise delay with a variable delay circuit; and

repeating the steps of delivering the first test signal, delivering the second test signal, placing the first edge, latching data, determining functionality, and varying the precise delay to determine maximum and minimum timing requirements of the logic element.